REMARKS

In response to the Office Action mailed November 10, 2003, Applicants thank the Examiner for allowance of Claims 10-17. However, Applicants respectfully request that the Examiner reconsider his rejection of the remaining claims.

Claims 1-17 have been elected without traverse and remain in the application.

Claims 18-35 have been withdrawn.

Claims 10-17 are allowed.

Claims 3-7 and 11 are being amended.

Claims 3-7 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention.

Applicants have amended Claim 3, as set forth above, to obviate ambiguities in the claim language. Specifically, Claim 3 has been amended to particularly point out that each of the two source registers holds first and second sets of bits, and that each of the first and second sets of bits is either signed or unsigned during a given operation. Applicant also respectfully points out that the "carry bits" are the conventional carry bits, which result during binary addition and multiplication operations, when the most significant bit of the input operands is exceeded.

Applicants have amended Claims 4 – 7 to correct the definition of the first and second sets of bits in the first and second source registers.

Claims 1-7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Kuroda, et al.* (U.S. Patent 4,722,068) (hereinafter "the *Kuroda* reference"). Applicants respectfully traverse these rejections.

Contrary to the examiner's statement that all elements are disclosed in the *Kuroda* reference, the *Kuroda* reference does not disclose a multiplier – accumulator. Specifically, the *Kuroda* reference only discloses, in FIGURE 8a as cited by the Examiner, a multiplier 22, an associated output register 224, and a following arithmetic logic unit (ALU) 32. FIGURE 8a of the *Kuroda* reference does not teach an

accumulator or the capability to perform an accumulation operation in the structure that is disclosed.

Contrary to the examiner's statement that all elements are disclosed in the *Kuroda* reference, the *Kuroda* reference also does not disclose input multiplexer circuitry for selectively presenting third and fourth operands to inputs of an adder and which selects the third and fourth operands from the contents of a set of associated source registers, the data output from a multiplier array, and the data output from the adder itself. Instead, multiplexer 31, identified by the Examiner in FIGURE 8 of the *Kuroda* reference, only selects one input operand being presented to one (i.e. the left) input arithmetic logic unit (ALU) 32. The right input to ALU 32 is provided directly from the output register file 26. Furthermore, multiplexer 31 only performs a two – to – one (2:1) selection between data output from multiplier 22 and data on bus 21, rather than a three – to - one selection. Thus, the rejections are unsupported by the art and should be withdrawn.

Claims 1-7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by *Tanoue, et al* (U.S. Patent 6,233,597) (hereinafter "the *Tanoue* reference"). Applicants respectfully traverse these rejections.

Contrary to the examiner's statement that all elements are disclosed in the *Tanoue* reference, the *Tanoue* reference does not teach input multiplexer circuitry for selectively presenting third and fourth operands to inputs of an adder and which selects the third and fourth operands from the contents of a set of associated source registers, data output from a multiplier array, and data output from the adder. In particular, in the system shown in FIGURE 1 of the *Tanoue* reference, each selector 18 and 19 only performs a two – one selection and only to a corresponding one of the two data inputs to adder 14. Specifically, selector 18 only selects between data on a first bus (unnumbered) and data output from adder 14 for presentation to the left input to adder 14. Selector 19 only selects between data on a second bus (unnumbered) and the output of multiplier 13 for presentation to the right input to adder 14. In other words, selectors 18 and 19 do not provide for the selection of one of three different data

sources to each input of adder 14. Thus, the rejections are unsupported by the art and should be withdrawn.

Claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being obvious over the *Kuroda* reference in view of *Landers, et al.* (WO 98/32071) (hereinafter "the *Landers* reference") Applicants respectfully traverse these rejections.

Contrary to the examiner's statement in the office action, Claims 8 and 9 are not taught or suggested by the *Kuroda* reference for the same reasons above that claim 1 is not taught by that reference. Similar to the *Kuroda* reference, the *Landers* reference does not disclose or suggest input multiplexer circuitry for selectively presenting third and fourth operands to inputs of an adder and which selects the third and fourth operands from the contents of a set of associated source registers, data output from a multiplier array, and data output from the adder. Specifically, the *Landers* reference only discloses, in FIGURE 3 as cited by the Examiner, a system in which the output of a multiplication – accumulate unit (MAC) 68 is directly presented to one input of an adder 70. Additionally, it appears that data output of adder 70 cannot be selectively fed-back through selectors 66 and 76 to two inputs of adder 70 itself. Thus, Claims 8 and 9 are not taught or suggested by the *Kuroda* and/or *Landers* references, either alone or in combination, since neither of these references discloses or suggests input multiplexer circuitry for selectively presenting third and fourth operands to inputs of an adder and which selects the third and fourth operands from the contents of a set of associated source registers, data output from a multiplier array, and data output from that adder. Thus, these rejections are unsupported by the art and should be withdrawn.

Claim 11 is being amended merely to correct a grammatical error.

The Specification is being amended to correctly identify the related applications and their current status.

No new matter has been added; the application has been merely amended to more particularly point out and distinctly claim the subject matter Applicant believes is inventive.

Applicant respectfully submits that the Claims as they now stand are patentably distinct over the art cited during the prosecution thereof.

With the addition of no new claims, no additional filing fees are due. However, the Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account Number 23-2426 of WINSTEAD SECHREST & MINICK P.C.

If the Examiner has any questions or comments concerning this paper or the present application in general, the Examiner is invited to call the undersigned at (214) 745-5374.

Respectfully submitted,
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